Printed Pages – 3   Roll No. : ....

B022314(022)

B. Tech. (Third Semester) Examination, Nov.-Dec. 2021

(AICTE Scheme)

(CSE Engg. Branch)

DIGITAL ELECTRONICS & LOGIC DESIGN

Time Allowed : Three hours

Maximum Marks : 100

Minimum Pass Marks : 35

*Note : Part (a) is compulsory and attempt any **two** parts from (b), (c) and (d).*

Unit-I

1. (a) Convert 10101001 in Gray code.   4

(b) State and prove Demorgan's law.   8

(c) Describe NAND and NOR gate as universal gate.   8

(d) For 7 bit hamming code received code is 1111101
find error use even parity.   8

Unit-II

2. (a) Define Fan in and Fan out.   4

(b) Describe CMOS NAND gate.   8

(c) Describe CMOS NOR gate.   8

(d) Describe TTL open collector circuit.   8

Unit-III

3. (a) Define the term Combinational Circuit.   4

(b) Describe full adder circuit with diagram and truth table.   8

(c) Design 4×16 decoder using 3×8 decoder.   8

(d) Implement the Boolean expression

$$F(A, B, C) = \Sigma m(0, 2, 5, 6)$$

using 4 : 1 multiplexer.   8

Unit-IV

4. (a) Define sequential circuits.   4

(b) Describe S-R flip-flop with diagram.   8

(c) What is race around condition and also describe
master slave flip-flop?   8

(d) Describe how to convert D flip flop into T flip-flop. 8

Unit-V

5. (a) Define state diagram.   4

(b) Describe Mealy State Machine.   8

(c) Describe Moore State Machine.   8

(d) Describe basic components of ASM charts.   8